Application of the active pixel sensor concept to guidance and navigation

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ABSTRACT

Char ~,c-coupled dc.vices (CCDs) have been used extensively in the past in star trackers and fine guidance systems. A new technology, the active pixel sensor, is a possible successor to CCDs. This technology potentially features the same sensitivity and performance of the CCD with additional improvements. These improvements include random access capability, easy window-of-interest readout, non-destructive readout for siglkal-lo-noise improvement, high radiation tolerance, simplified clocking voltages, and easy integration with other on-chip signal processing circuitry. The state-of-the-art of this emerging technology and its potential application to guidance and navigation systems is discussed.

1. INTRODUCTION

Spacecraft guidance and attitude control systems today typically employ a set of celestial sensors to establish the spacecraft's orientation with respect to a planetary body or the fixed inertial frame provided by the sun and stars. In many cases this set includes a star tracker capable of providing two- or three- axis attitude information by determining the centroids and thereby establishing the relative position if one or more guide stars within its field of view.

"1 'racker characteristics a ad operat ions tend to be strongly mission-dependent. The upcoming Cassini mission to Sat urn requires a tracker capable of providing four ale-second pointing accuracy by tracking three stars of magnitude 5.8 or bright er over a 15-18 degree field-of-view. Mass of the tracker is to be no more than nine kilograms and power consumption is not to exceed 12 watts. In contrast, preliminary studies of a Pluto fly-by mission suggest the tracker's pointing accuracy can be relaxed to 40-arc seconds, but it must now weigh no more than 0.5 kg and consume less than 5 W.

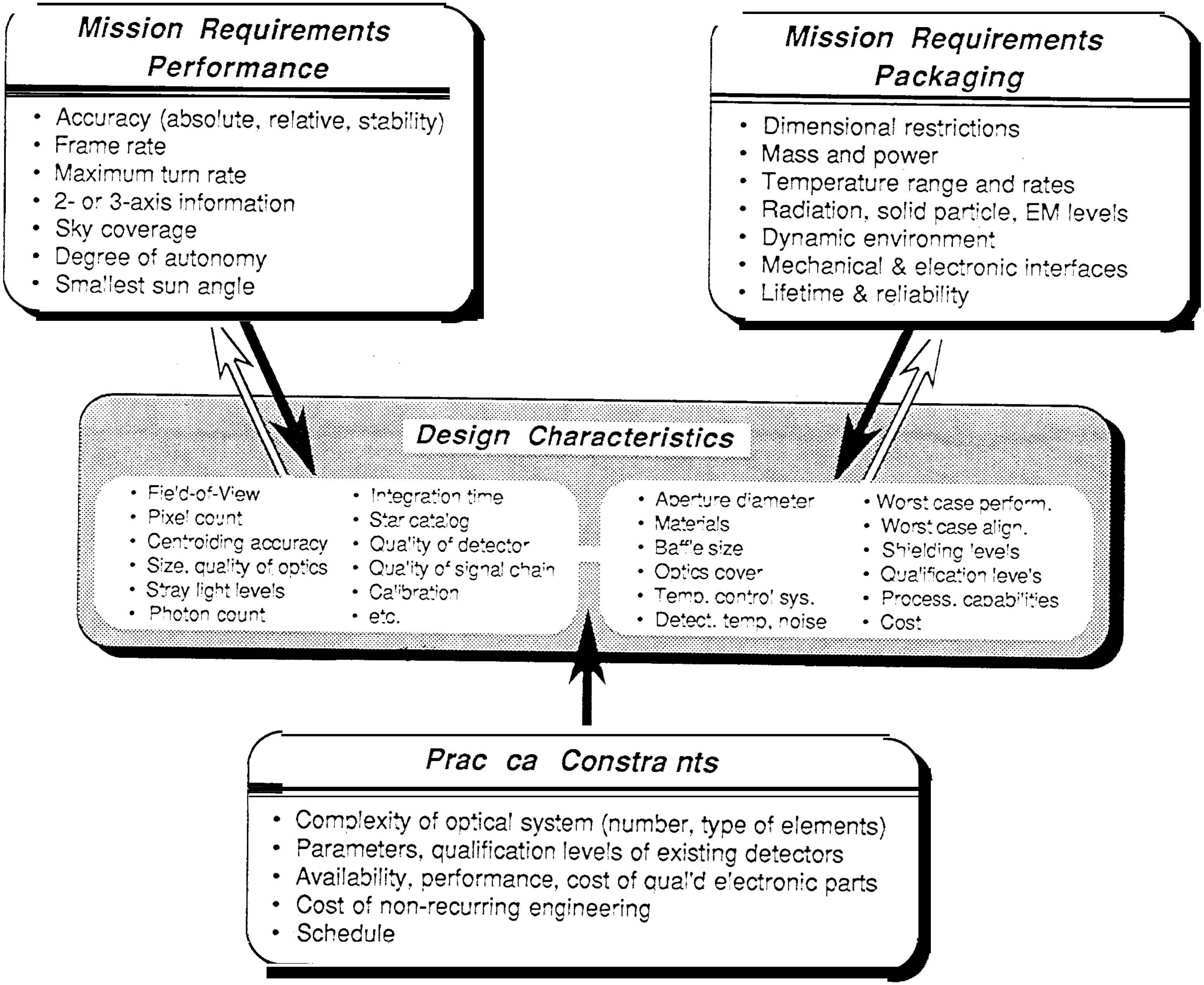
Selection, modification or design of a star tracker is thus a matter of identifying, weighing and often compromising among a number of competing requirements and constraints, as indicated schematically in Fig. 1.

In many instances, a small number of the requirements or practical constraints arc very tightly restricted and thus define the starting point for the selection/design process. Given the highly coupled, interactive nature of the requirements, constraints and their physical manifestations, this process often involves a number of iterations before an acceptable solution appeals,

The one unifying theme for the current generation of star trackers is the usc of a two-dimensional CCD focal-plane array, usually containing on the order of512xS12 pixels. During the late 1970's and early 1 980's, low noise, high sensitivity, wide dynamic range CCDs were developed for scientific imaging applications[1,2]. It soon became apparent that the CCDs' combination of control flexibility and performance attributes made it an attractive alternative to image dissector tubes as the basis for imaging star trackers[3,4,5,6,7,8].

(El) 's, though, arc not without problems or limitations. The Achilles' heel of CCD technology is fundamental to its operation -- the need for the perfect transfer of charge across macroscopic distances through a semiconductor. Although CC1)s have become a technology of choice for present-day implementation of imaging and spectroscopic instruments, it is well-known that they are a particularly difficult technology to master. The need for near-perfect charge transfer efficiency makes CCDs (1) radiation "soft," (2) difficult to reproducibly manufacture in large array sires, (3) incompatible with the on-chip electronics integration requirements of miniature instruments, (4) difficult to extend the spectral responsivity range through the usc of alternative materials, and (S) limited in their readout rate. A new imagi ng sensor technology that preserves the positive attributes of the CCD yet eliminates the need for charge transfer could quickly eclipse the CCD.

Tracker Specification and Design: An Interactive, Iterative Process



In this paper, the active pixel sensor (APS) technology is discussed. The application of APS technology to the needs of guidance and navigat ion start rackers is considei cd and the potential advantages of the APS technology arc explored.

2. THE ACTIVE PIXEL SENSOR CONCEPT

Continued advancement in microlithography feature size reduction for the production of semiconductor circuits such as DRAMs and microprocessors since the invention of the CCD in 1970 enables the consideration of a new image sensor technology, called the Active Pixel Sensor (APS)[9]. *In the new APS concept, one or more active transistors are integrated into the pixel of an imaging detector array, and buffer the photosignal as well as drive the readout lines.* At any instant, only onc row's transistors arc activated, so that power dissipation in the APS is approximately that of the CCD. The physical fill-factor of the APS can bc approximately 50% or higher, and the usc of on-chip microlenses or binary optics can increase the effective fill-factor to over 80%. Sensitivity, read noise, and dynamic range arc similar to the CCD. Thus, the APS preserves the high performance of the CCD but eliminates the need for charge transfer.

There arc a multitude of ways to implement an active pixel sensor but there arc primarily two types, lateral APS structures and vertical structures. In the lateral structure, the photosite is adjacent to the readout transistors. This structure simplifies the fabrication process and allows somewhat separate optimization of the photodetector and readout transistors. The penalty for this latitude is a reduction in effective till factor. In the vertical APS structure, the photodetector is vertically integrated with readout transistor(s). By stacking the these devices together, the pixel size can be reduced and the effective fill factor remains high.

A simple example of an active pixel is illustrated below. In this example, a lateral APS structure that resembles a short CCD is shown. Charge is integrated under the photogate PG. To read out the signal, the pixel is selected using transistor S. The output node is reset using transistor R. The signal charge is then transferred from under PG into the output node. The change in the source follower voltage between the reset level and final level is the output signal from the pixel. The source follower might drive a column line terminated with clamp and/or sample-hold circuits. These colu]nn-parallel circuits can then be seamed for serial readout of the sensor. Since the illustrated APS requires only a single int ra-pixel charge transfer, many of the problems associated with charge transfer in CCDs arc eliminated.

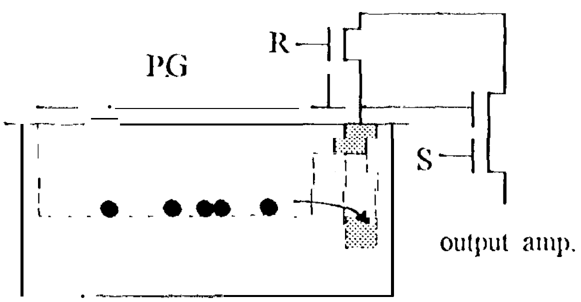


Fig. 2, Schematic illustration ofa lateral APS pixel.

J} '1, is exploring this type of structure fabricated in standard foundry CMOS technology. A **40x40** micron pixel configured in a 28x28 array was designed, as shown below, Row and column decoders were formed using standard CMOS digital logic. The *sensor* was addressed a tow at a time. The reset level and signal level were captured using two sample and hold circuits. The output of these circuits was scanned by sequentially addressing the columns. The image sensor was fabricated by a foundry and tested at JPL. Operation requires the input of digital X and Y pixel addresses as well as pulsing the photogate and sample/hold gates. All input signals were TTL compatible, e.g. O and 5 volts. The image sensor was operated at a pixel rate of approximately 0.5 megapixel/sec. The charge to volts.gc conversion rate was estimated to bc 4.0 μV/electron with a saturation level for this surface-chaanc] device of approximately 600 mV. Fixed pattern noise was observed to bc approximately 1.5% full-scale and can likely be reduced by an order of magnitude by improved on-chip signal processing. A layout of the pixel used in the experimental sensor is shown below. While this device used destructive readout with a floating diffusion sense amplifier, a non-destructive float ing-gate sense amplifier has also been demonstrated. Further efforts using standard CMOS arc aimed at demonstrating a camera-on-a-chip for usc in future microspacecraft applications. The camera-on-a-chip will include an on-chip A/D converter[10] 10 allow a full digital interface with external circuitry.

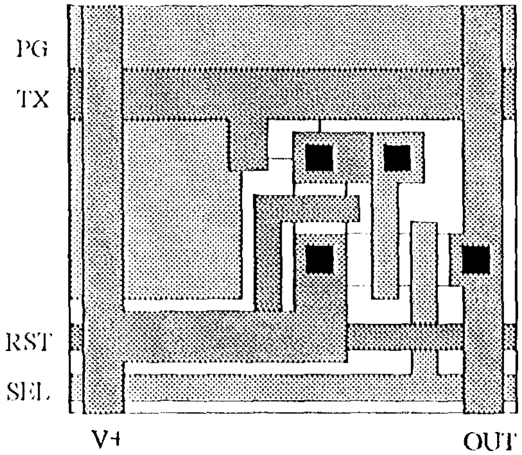


Fig. 3. Schematic layout of the JPL CMOS AI'S. Fill factor is approx. 25%.

Much more sophisticated active pixel structures arc being pursued elsewhere in order to achieve small pixel size rind high fill factors. For example, Toshiba is using its double-~atc floating surface transistor to increase the sensitivity of the output amplifier to 200 μV/electron [11]. To reduce the pixel size, the charge storage area can be located vertically under the (or over) the readout transistor. The presence or absence of photo-generated charge can bc used to modulate the readout transistor output signal. This approach is used by Olympus in its charge modulation device (CMD) approach to active pixel sensors [12]. Texas Instruments (Japan) is using a bulk charge modulated device (BCMD) in a hexagonal packing format [13]. A further reduction in pixel size can be enabled if the current flow in the output transistor is vertical rather than horizontal so that the substrate acts as onc of the transistor terminals. This approach is used by Olympus in its static induction transistor (S1"1') AI'S device [14]. A vertical bipolar approach is used by Canon in its base-stored image sensor (BASIS) [15]. These technologies arc all non-destructive in their readout of the pixel allowing multiple sampling of the photosignal for improved SNR

The fill factor of APS technologies arc generally smaller than that of full-frame CCDs. The usc of on-chip microlenses, already incorporated in commercial interline CCD products (e.g. Sony, Kodak) can be used with AI'S devices to bring their effective fill factor to same level as a full-frame CCD. The microlense concept is shown below.

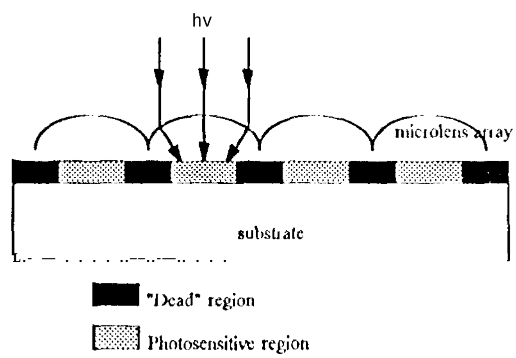


Fig. 4. Schematic illustration of on-chip microlens array to increase effective fill-factor.

Each of these technologies has its own set of advantages and disadvantages. Fixed pattern noise is generally a common concern but can be eliminated through on-chip signal processing. The fixed pattern noise. arises due to threshold voltage non-uniformities across a large area image sensor, Since output amplifiers track the threshold voltage of the output transistor, the APS is sensitive to this offset pattern. Clamp circuits can be used to nearly eliminate this phenomenon, At the present time, only the JPL APS is 100°/0 CMOS compatible. However, many of the other technologies arc amenable to integration with CMOS (unlike the case with CCDs) and thus enable the consideration of low-power, low-voltage on-chip electronic circuitry.

3. APPLICATION OF THE APS CONCEPT TO STAR TRACKERS

In discussing the application of APS technology to star trackers, it is assumed that the APS technology is a CMOS-compatible technology. There arc two aspects of AI'S technology that make of particular importance to star tracker application, these arc customization and miniaturization. In addition, the potential for in-pixel processing allows the consideration of significant evolution in the realization of star trackers.

3.1 Customization

Many applications demand long lifetime, high reliability star trackers, This places similar demands on the tracker components, notably the detector array and the associated drive and processing electronics. Traditionally, these reliability requirements have dictated the usc of a rather select list of space-qualified parts. To achieve their space-qualified status, these parts have undergone extensive test and analysis, as evidenced by hundreds of pages of careful documentation. Not surprisingly, the costs of qualifying a new part can easily run several hundred thousand and even well over a million dolla Is. Consequently, the list of available fully qualified (so-called Class SA) parts is comparatively small and generally represents somewhat dated technology.

As might be expected, the list of qualified CCDs reflects the above problems: it is neither extensive nor particularly representative of the current CCD s(atc-of-the-ar(. Despite the fact that 4096 x 4096 pixel CCDs first appeared in the 1 iterature several years ago[16] and that 2048 x 2048 arrays arc now commercially available, no star tracker yet flown has employed an array of more than 512 pixels 011 a side. The first trackers to employ a 1024 x 1024 array, e.g. those to be used on the Cassini mission, will not be flown until some time in 1997.

The need to "make do" with a small and dated parts list manifests itself in performance, power consumption and/or mass significantly worse than might be realized with state-of-tbc-al-t components. These shortcomings arc further magnified in the case of centerpiece devices such as microprocessors or CCDs, whose limitation arc necessarily propagated through a cast of supporting and peripheral parts.

Application-Specific Integrated Circuits or ASICs, Field-Programmable Gate Arrays and related devices appear to be on the verge of both expanding and updating the electronics side of the parts list. In some sense, these devices represent qualification of a process, i.e. a library of subelements, connection rules, materials and fabrication procedures, rather than a specific part.

APS technology could do the same for detector arrays. A qualified AT'S library would allow designers to optimize a sensor for their application rather than adapt their application to make usc of onc of the few available sensors, A set of small, application-specific changes to an existing sensor, unthinkable in the context of the associated requalification costs for an otherwise available CCD, could easily be implemented in an ASIC-like APS array. And, apart from the non-recurring engineering **costs** associated with any new design, a completely new, application-specific, flight-ready APS array could be purchased for little more than the cost of an existing device based on the same AT'S process,

In principle, a similar argument might be attempted on behalf of CCD technology: could not an ASIC-like CCD process be dc}'eloped and qualified? Perhaps, but one is again confronted with both the rather difficult, narrowly-focused nature of CCD device technology and the C'1'E-related design, processing and radiation sensitivity of CCDs. Whereas the CMOS VLSI technology of ASICs and AI'S devices has applications sufficiently numerous and widespread to support "silicon foul~dl-its" specializing in limited production of custom designs, the technology for reliable fabrication of high-performance CCDs is quite specific to CCDs. Further, given the CCD's CTE-driven sensitivity to change of design or environment, ii's not immediately clear how one would go about constructing a usefully flexible set of ASIC-like CCD design rules. In the absence of a very comprehensive test and analysis program, how could one be assured that even a seemingly small change in a CCD array would not have a significant negative impact on device performance or reliability?

3.2 Miniaturization

APS compatibility with CMOS VLSI will also allow a significant amount of the supporting control and processing electronics to be integrated on-chip with the detector array.

Examples of this high-level integration have already appeared in the literature. The Multi-port Array photo-Receptor system or MAR sensor[17] incorporates several shift registers, an analog multiplexer and decoder buffers with a 128 x 1 ? 8 APS array of hexagonal pixels. Mendis, et al.,[18] describe a chip that integrates a 128 x 128 APS array with a set of row and column select/drive electronics, a digital multiplexer and a set of 128 siglna-delta analog-to-digital converters.

VLSI Vision Ltd. (VW,) has recently announced a commercially available camera-on-a-chip, based on technology developed at the University of Edinburgh[19]. A 312 x 287 pixel sensor array is integrated with analog and digital circuitry, including automatic exposure and gain control, to generate a standard monochrome output signal. The unit, known as the Peach, measures only 35 mm in diameter across its housing and draws only 40 mA under a 7S ohm load from a regulated 7-10-1 ? VDC external supply.

These and similar developments indicate the size, as well as accompanying mass and power, reductions possible with APS technology. Such reductions will be increasingly important as the trend toward spacecraft downsizing continues: whereas the Voyager spacecraft stood some S meters tall and weighed over 800 kg, and Cassini will stand over 6 meters and is projected to weigh roughly 2150 kg dry, studies for a Pluto Flyby mission have suggested 1 meter tall spacecraft with a wet mass of perhaps 150 kg.

The higher level of on-chip integration will also reduce the number of external interfaces and amount of wiring required, which may in turn have a positive impact on reliability.

3.3 111-pixel signal conditioning/processing

By definition, APS devices incorporate one or more active transistors within each pixel. As a result, each pixel is able to condition and perhaps even perform limited processing on its received photosignal. This simple ability has the potential to dramatically alter the implementation of a number of existing functions and to open the door to a wide range of new possibilities.

Simplified windowing

After acquiring, and identifying the requisite number of stars, trackers will generally switch to a windowing mode of operation[4,6]. In this mode, each of the selected guide stars is enclosed in a window containing, a relatively small number, e.g. 5 x S, pixels. This allows a CCD tracker to clock rapidly through the vast majority of unimportant pixels, usually at rates of megapixels per second, slowing only when a critical date-bearing window pixel is encountered. Window pixels are read and digitized at a much slower low-noise rate, 011 the order of' 50,000 pcr second. Thus, a megapixel-class CCD can be read out, without compromising significant data content, in less than a tenth of a second as compared to the 10 or more seconds that would be required if the entire read-out occurred at the lcw-noise digitizing rate.

Nonetheless, it remains necessary to clock out all the CCD pixels in order to reach the few that are of interest and to switch back and forth between high-and low-speed read-out protocols as portions of various windows are encountered. This requires both power and coordination, Moreover, thousands of low-loss charge transfers must still be effected through fixed one-way paths to move photogenerated charge from a window pixel to the CCD's output amplifier.

As discussed earlier, in-pixel active elements allow random access to each pixel of an APS array and thereby completely eliminate the above issues. Individual windows can be accessed and read out as blocks in a repetitive process, simplifying both the control and data storage functions. Pixels outside the windows are left undisturbed. Charge transfer efficiency and the possibility of "blockages" are inherently non-issues because no charge is being transferred.

Posit ion-specific exposure control

Exposure time for a CCD is generally determined by a desire that the. brightest significant pixel in the array contain a full well of photoelectrons. Less than a full well represents a (presumably) unnecessary sacrifice of sigila]-to-noise ratio and, with it, centroiding accuracy. More than a full well, or blooming, produces a decidedly nonlinear plateau in the pixel's photoresponse and may also result in excess electrons spilling over into adjoining pixels. Once again, this has a negative impact on centroiding accuracy.

Of course, if the brightest pixel contains a full well of electrons, other pixels will contain significantly less and will therefore exhibit reduced sigual-to-noise ratios and poorer centroiding accuracies. This means that either the tracker field-of-view must be sized to assure that the required number of tracked stars all are toughly comparable in magnitude or that other tracker parameters must be chosen so that the degraded centroid / attitude determination accuracy associated with dimmer guide stars is nonetheless sufficient to fulfill the specified pointing requirements.

Again, APS arrays may well bc able to avoid these restrictions by allowing Positioll-specific exposure control. For example, in the windowing mock, exposure control could bc effected on a window-by-window basis. This control is enabled by the]andom-access, non-destructive mad-out characteristic of AI'S pixels.

Simplified pixel summing for multi-resolution processing

These same characteristics can significantly simplify the process of pixel-smming often associated with data compression and/or multi-resolution imaging. Pixel-sulnming is simply the addition, either analog or digital, of the contents of two or more adjoining pixels, resulting in a lower resolution, but more compact representation of the image captured by the detector array.

The destructive nature of a CCD read-out dictates that pixel-summiug bc either a repetitive analog process, involving as many exposures as summing levels, or a digital process in which the full image as well as the results of successive summing filters are stored in digital memory. No(c that this type of processing essentially requires that the entire CCD be read at the time-consuming, low-noise digitizing rate.

In contrast, the non-destructive, random-access nature of APS read-out allows the sensor array to serve as its own high-resolution image buffer and thereby support repeated, multi-resolution analog or digital processing of the data obtained in a single exposure. The APS thus enjoys the benefits of the CCD digital process without incurring the CCD's speed or memory penalties,

Simplified and/or accelerated "blob" identification

l'rackers are generally designed to spread the image of a star over several pixels to allow sub-pixel centroid determination, often at the level of 0.1 to 0.01 pixels[4,6]. A star image confined entirely within a single pixel would restrict the centroid resolution to ±1/2 pixel.

"Blob" identification is the process of collecting data from adjoining pixels to determine the approximate locations and boundaries of contiguous objects within the, detector's field of view. in the context of star trackers, this is basically a matter of sorting pixels into "haves", which contain more than a certain number of photoelectrons, and "have nots" and then identifying groups of adjoining "have" pixels as potential star images. One is also well-advised to make certain that a blob is not indeed a blob, i.e. an extended object such as a planet or a star cloud, which is likely to confuse the tracker's star idc]l[ifica[ion/attitude determination software.

In a CCI)-based tracker, the have or have not data for blob identification can be obtained by applying a threshold to a full-frame pixel-by-pixc] read-out of the CCD. Locations of "have" pixels arc stored in memory for usc by the blob algorithm.

An AI'S array may offer simpler and/or faster approaches to blob identification. For example, the simplified pixel summing capabilities of an APS array could bc exploited by using a coarse (perhaps 32 x 32) summing filter to scan the array for brighter-than-average areas and then applying successively finer filters within those areas to identify blobs.

New or improved capabilities enabled by flexible pixel and/or array geometries

The "bucket brigade" nature of CCD charge transfer militates in favor of a rectangular cells. Significant variations in ccl] size or form factor would produce corresponding variations in apparent photosensitivity and/or charge transfer efficiency c.g. a smaller cell would clip the attempted transfer of a full well from a larger cell). High uniformity in the cells' form factors in therefore critical in high-performance CCDs. This need for high uniformity, combined with the simple geometrical fact that only triangles, rectangles or hexagons can bc used to repetitively tile a plane, all but dictates the use of rectangular cells and arrays.

There are, of course, exceptions to this rule. Annular geometry CCDs, comprised of a single ring of uniform arc segment cells, are commercially available. However, these arc essentially linear rather than two-dimensional arrays and are therefore of little interest in the context of this discussion. "Log-polar" CCDs, realized as concentric 64-segment rings of exponentially increasing width, have been developed by Univ. Penn[20]. These arrays pay for their non-uniform cell structure by subdividing large cells into smaller, more compatible ones, arranging the output shift register so that the largest cells are closest to the output and therefore are not clipped in the transfer process, varying the A/D gain as a function of readout position, etc..

Random pixel access and independently controllable pixel gains make it possible for APS detectors to use non-rectangular, variable geometry pixels arranged in non-rectangular, non-uniform arrays. As noted above, the MAR sensor employs regular hexagonal pixels[17]. In that particular application, the hexagonal pixel geometry facilitates the use of circularly symmetric operations such as the Laplacian or difference of Gaussians, often used to provide edge extraction in image processing schemes. Hexagonal pixel arrays have also been shown to be superior to rectangular arrays in centroiding applications[21] as manifested by reduced error levels (as much as a factor of three), reduced noise sensitivity and reduced computational and storage requirements.

New or improved capabilities enabled by in-pixel processing

As star trackers evolve into more versatile instruments, capable of identifying and tracking not only stars but also planetary features, they will radically alter the manner in which science instruments are pointed and controlled. Pointing will be based on objects of interest rather than inertial coordinates, eliminating many time-consuming, fuel-wasting maneuvers as well as the deluge of extraneous information that has heretofore accompanied the date of interest,

Feature recognition and tracking capability will, of course, require image processing capabilities more akin to those of a human being than to a high-resolution camcorder. As CMOS VLSI fabrication processes continue to improve, it will be possible to place additional processing elements inside each without diminishing their fill factors or other important optical/optoelectronic properties. This will open the door to in-situ analog processing the incoming, photosignals, allowing the APS array to mimic some functions of the human retina.

Work in this area is already underway. Caltech has developed and tested a number of "artificial" or "silicon" retinas, featuring in-pixel logarithmic and differencing amplifiers and resistive network connections to adjacent pixels[22]. These simple features have allowed the silicon retina to exhibit a number of the characteristics of human retinas, e.g. edge extraction, adaptation to stationary images/accentuation of moving objects and susceptibility to certain types of optical illusion,

There are many issues that JPL has just begun to explore regarding the use of the active pixel sensor in a star tracker, and definitive conclusions have not yet been reached. Some of these issues are the effect of a reproducible and regular, but odd-shaped photoactive region on the centroiding process, the optical effect of metallic wires running over the surface of the imager, and the effect of microlenses on the centroiding algorithm. While none of these issues are APS technology show-stoppers, they are important to the analysis of any imaging system using APS technology.

4. CONCLUSIONS

The active pixel sensor concept has been presented. Work on this technology is proceeding in several companies and at JPL, though the centroid of the work is in Japan. In just the few years that have elapsed since this technology has been explored, rapid improvement has been demonstrated to the point where the future of CCDs is called into question, The possible applications of the APS technology to star trackers has been discussed, While the discussion is presently speculation, it appears that there is a wide opportunity for APS technology to benefit the star tracker community. JPL is continuing its efforts to better understand APS technology developed in industry, as well as *explore* CMOS APS structures and their application to guidance and navigation.

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